AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF CLAIMS:

Claim 1 (currently amended): A CMOS register circuit having a plurality of n-channel MOSFET transistors and a plurality of p-channel MOSFET transistors, accepting an input data, and a clock signal, and providing an output data, said clock signal not being a conventional CMOS signal and instead being a charge recycled clock signal having a stepwise waveform from a switched capacitor regenerator ~~or sine waveform from an LC resonant circuit~~ in which power supplied to a load is at least partially collected to said switched capacitor regenerator ~~or said LC resonant circuit~~, and

the following inequality is satisfied[[;]] for getting rid of short circuit current:

$| V_{TN} | + | V_{TP} | \geq VDD$

where V_{TN} is a threshold of said n-channel MOSFET transistor, V_{TP} is a threshold of said p-channel MOSFET, and VDD is an output voltage of said switched capacitor regenerator ~~or said LC resonator circuit~~,

wherein said register circuit comprises a pair of D-latch circuits with an input of a second D-latch circuit coupled with an output of a first D-latch circuit, a first D-latch circuit accepts a first [[power]] stepwise waveform clock signal, and a second D-latch circuit accepts a second

[[power]] stepwise waveform clock signal which is different by 180° phase of the first power clock signal.

Claim 2 (currently amended): A register circuit according to claim 1, wherein said D-latch circuit comprises a pair of NOR circuits with one of the inputs of each NOR circuit being coupled with an output of the other NOR circuit, and a pair of AND circuits each accepting an input data in differential form and a [[power]] stepwise waveform clock signal, and providing an output to the other input of each of said NOR ~~circuit~~ circuits.

Claim 3 (original): A register circuit according to claim 1, wherein said D-latch circuit comprises a memory element having a first inverter providing an output of the D-latch circuit, a second inverter with an input coupled with an output of said first inverter, and a first transmission gate connecting an output of the second inverter to an input of the first inverter, and a second transmission gate inserted between an input terminal and an input of said first inverter.